Diyala Journal of Engineering Sciences, Vol. 11, No. 2, June 2018, pages 60-66 ISSN 1999-8716
DOI: 10.24237/djes.2018.11208 eISSN 2616-6909

A New Technology for Reducing Power Consumption in Synchronous Digital Design Using Tri-State Buffer

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Abstract: This research paper deals with design and implementation of low power 8-bit arithmetic logic units. The main part of power consumption is consumed in ALU in any processor. Therefore, reducing power dissipation in ALU should be requiring. The proposed technique disabled one of the main block of ALU using tri-state logic which is not necessary to use, except the required processes. In this work, the suggested design is realized by using ASIC methodologies. In order to implement the arithmetic and logic architectures, 130 nm standard cell libraries are used for ASIC execution. The architecture of the design has been created using Verilog HDL language. In addition, it is simulated using ModelSim-Altera 10.3c (Quartus II 14.1) tools. By using tri-state technique, dynamic power and total power are decreased.

Keywords: ALU; Tri-state logic; Dynamic power consumption.
Paper History: Received: (9/4/2017), Accepted: (25/9/2017)

Introduction

In modern time, power dissipation is a necessary term for all chip designers. Basically, any design consumes power in two types, first is dynamic power consumption and second static power. Where, the static power due to leakage current while the dynamic power consumption due to internal switching of the capacitance [1]. Clock power consumes the main part of the power wasted in ALU. There is more than one way to reduce power dissipation in the system. In this research paper, dynamic power and total power consumed are reduced in the circuit. An 8 bit ALU is designed and powers optimization are achieved by the help of tri-state logic. The size of an ALU can be easily modified by 16-bit, 32-bit and 64-bit. Power dissipation is estimated by the factors called dynamic power, short circuit power and leakage power including the parameters that used to estimate total power consumption like frequency, switching activity, supply voltage and capacitor [2]. Power consumption equation is given as:

$$P_{total} = P_{leakage} + P_{dynamic} \quad (1)$$

The main part of power consumption dynamic power is switching power defined as [3]:

$$Pdynamic = \alpha * C * V^2 f \quad (2)$$

From equation 2; α is the switching activity measured in *Mw*, *C* is the capacitor measured in *Mf*, *V* is the supply voltage and *f* is the frequency measured in *MHz*.

Literature Review

The research surveys clearly indicate that the scale of power optimization is high at the system level than at the transistor level [4] (Kathuria, et al., 2011). In this work, the designer applied a new technology for low power techniques at the architecture level of ALU. The design is verified by applying clock gating signal using tri-state logic. The ALU design is the synchronous systems which apply with the clock input. The clock signal in synchronous design consumes much power. From previous works, the clock consumes power up to 30% of the total power [5] (Pandey & Pattanaik, 2013), [6] (Brynjolfson & Zilic, 2000). In the same way of power reduction, [7] (Soni & Hiradhar, 2015) presented a review on the existing clock gating techniques and produced a similar study of those clock gating in synchronous circuit like ALU. Then, a new technique for clock gating which will provide more immunity to the current problem is obtained from the existing techniques.

In the previous works, all reduction power techniques were facing with the problem of size. Those methods which required less size had problem in other area like glitches while those approaches that required large size did not have glitch problem but increase static problem. In all the previous techniques, only few approaches could reduce the clock. As the involving of tri-state technology, [8] (Maan, et al., 2017) used an effective technique of decreasing dynamic power dissipation in synchronous design. In this work is presented a comparative analysis of an 8-bit ALU. The designer is generated a circuit used tri-state buffer in a negative latch design, instead of OR gate logic. With the same function being performed, this circuit saved more power and reduced utilized area, irrespective of design performance. The minimum power gain realized 6.4 % percentage of total power consumption by executing 20 MHz frequency. Therefore, the demand to decrease this power is a difficult task for the researchers. Tri-state logic is applied to the design with power analysis for each scale of frequency.

1. Implementation of ALU

This research paper presents an 8-bit ALU. The inputs *a* and *b* are of 8- bits and the result is also an 8-bit. The ALU is executed as two functional blocks, Logical and Arithmetic units. Arithmetic unit performed all arithmetic operations. Moreover, logical unit performed all logic operations. The design utilized selects lines

every one for unit module. The sel [2:0] signal is used to select the required operation. On applying the clock signal, based on the select lines, two inputs are evaluated and the result is present at ALU_out. The operations are selected depending on various select lines are shown in the table 1. 8-bit ALU design is shown in figure 1. The ALU represented as two blocks, is executed using both with and without tri-state. ALU design is simulated using ModelSim-Altera 10.3c (Quartus II 14.1) and implemented by 130nm technology library [9].

Table .1: Select Line Operations

S2	S1	S0	Operations
0	0	0	AND
0	0	1	NAND
0	1	0	NOR
0	1	1	BUFFER A
1	0	0	SUBSTRACTION
1	0	1	DECREMENT
1	1	0	ADDITION
1	1	1	CLEAR

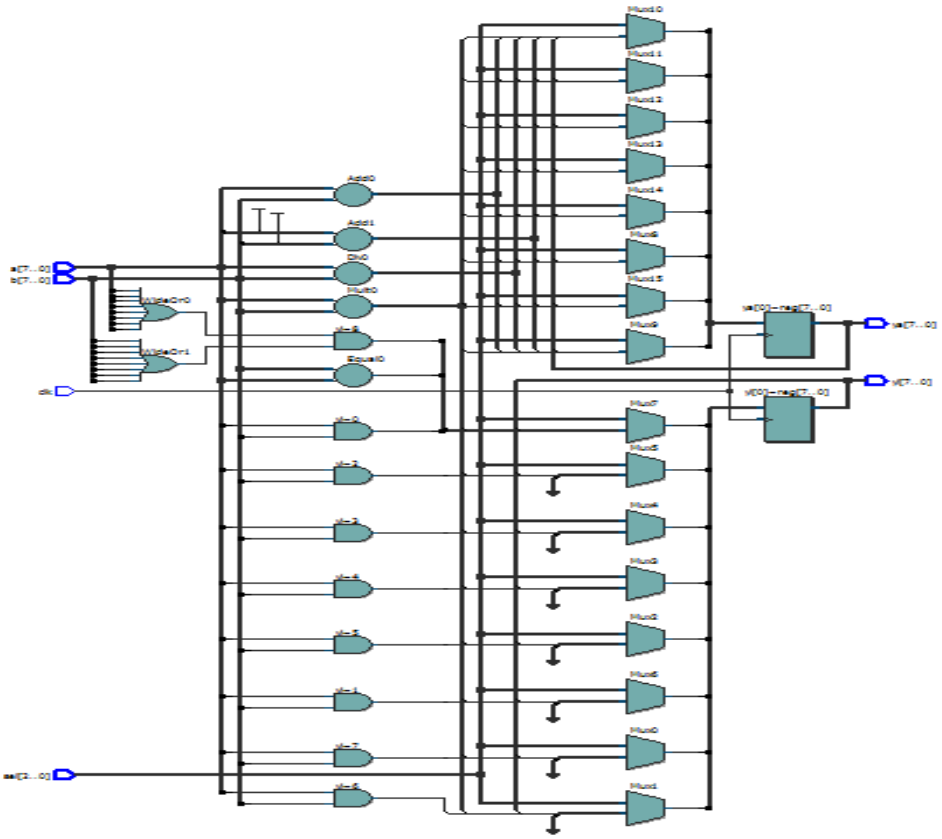


Figure .1: RTL Viewer of ALU design

2. **Tri-State Logic**

This section explains the way of low power 8-bit ALU design using tri-state buffer. With the help of tri-state logic, significantly reduced the dissipated of dynamic power. Basically, Tri-state logic is act as a switch. It is controlled by control signal, named as enable signal (en) as shown in figure. In tri-state buffer if en=1, that led to appear the input data at the output of tri-state buffer. In other word, the value of the input is equaled to output value (X=Y). But if en=0, then it acted as an open circuited and the input is disconnected to the output. Also, input value wouldn't appear at the output. Clearly, the process details are shown in figure 3. In this work, the property of tri-state buffer is used to decrease the power dissipation of 8-bit ALU [10]. It performs various processes during the executing in modules block. At one particular time one process performed [11]. While, all other processes (which are not select), consumes clock power at the same time. This will lead dynamic power dissipation.

The problem is overcome with the use of tri-state buffer. Therefore, at the time one process can perform by ALU, while all other operations are in tri-state high impedance Z state. In this case, it is possible to implement circuit with the help of tri-state logic. That leads to perform only one operation at one plus time, which is selection input for selected the target process [12]. Moreover, the other operations are remaining in high impedance Z state. In the other word, these operations cannot

access to output or connect to the output. The path of passing clock signal in different cases is presented in figures 4 and 5 respectively.

The way of execution using tri-state logic is shown in figure 4. Where, the implementation processes with tri-state as the way of clock signal. If en =1, then clock signal will be appearing at the clk_t1 output. But when the en signal set to 0 as shown in figure 5, clock input will be appearing at the clk_t2 output because an inverter makes en input 0 to input 1. So it acts as open circuited path [13]. This will ensure that ALU modules operations, only one module is selected at a time and performed, while rest of operations are in tri-state. In figure 6, the technology map viewer of tri-state circuit. While, the RTL viewer of tri-state logic technology as drown in Verilog HDL is presented in figure 7.

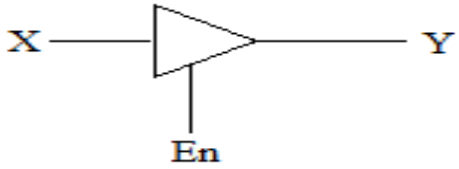
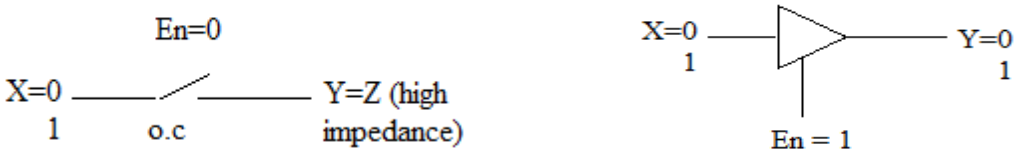


Figure .2: Tri-state logic diagram



(a) (b)

Figure .3: (a) when en=0 (b) when en=1

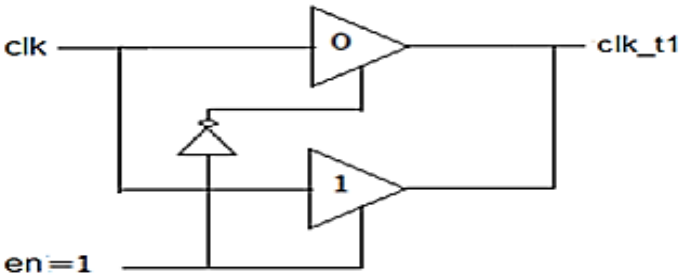


Figure .4: The path of clock signal using tri-state buffer when en=1

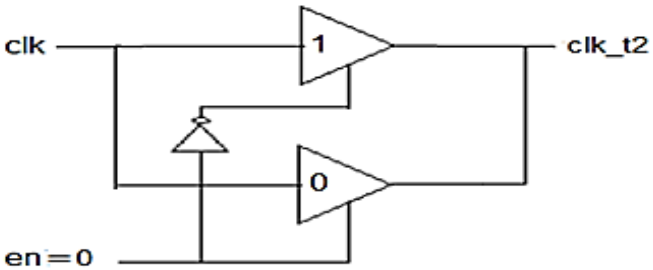


Figure .5: Clock signal flow using tri-state buffer when en=0

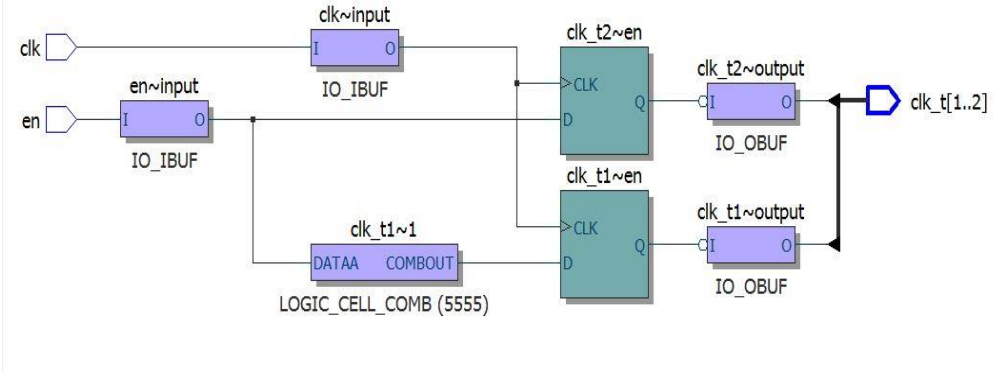


Figure .6: Technology map viewer of tri-state circuit

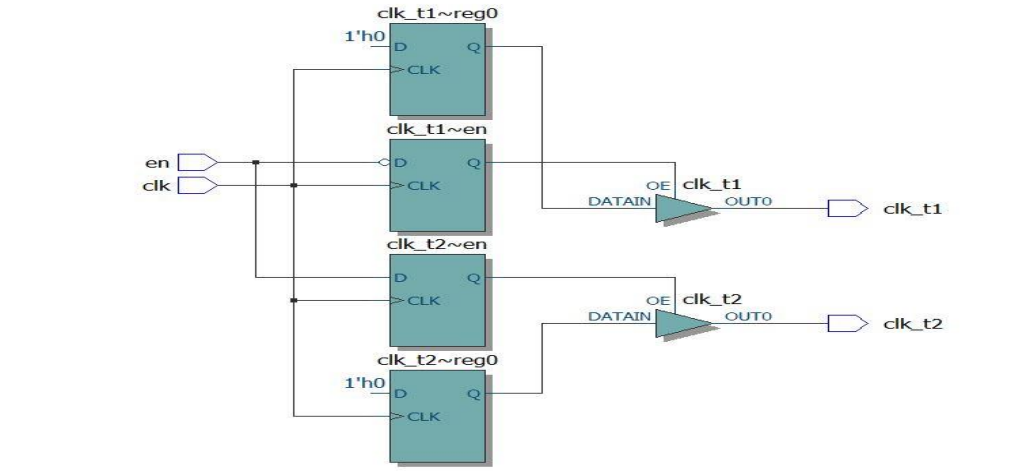


Figure .7: RTL viewer of tri-state logic technology

3. Validations and Results

Quartus II 14.1 (64-bit) Web Edition is used to implement ALU with 130 nm technology libraries used to perform power analysis. ModelSim-Altera 10.3c (Quartus II 14.1) is used to perform behavioral simulation and validation [4].

A- Behavioral Simulation

Validation software is used for the behavioral simulation and tested the ALU design with different values of input and in all conditions. ALU design is behaving as per the specifications. Figures 8, 9 and 10 show the behavioral of the waveform simulation of ALU with and without new tri-state logic design, in addition to the behavioral of tri-state design. Clear to observe that, how the new circuit switches had one process ON and other process OFF depending on the clk_t1, clk_t2. Figure 10 shows the validation of the input and output signals for ALU with tri state logic technique.

Figure .8: ALU waveform validation of ALU without tri state logic

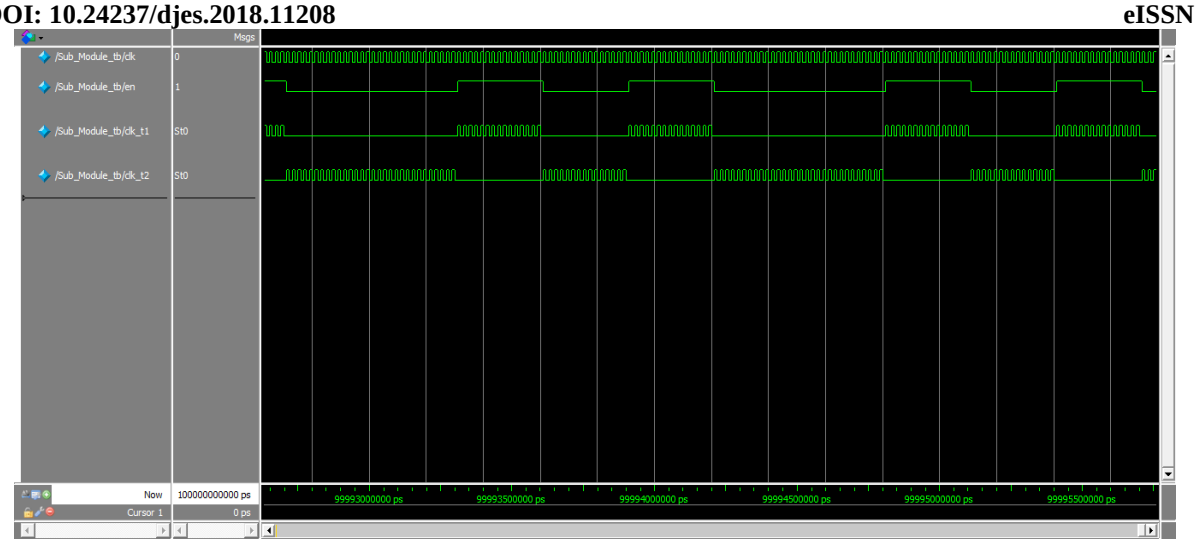


Figure .9: Simulation of the new tri-state logic design

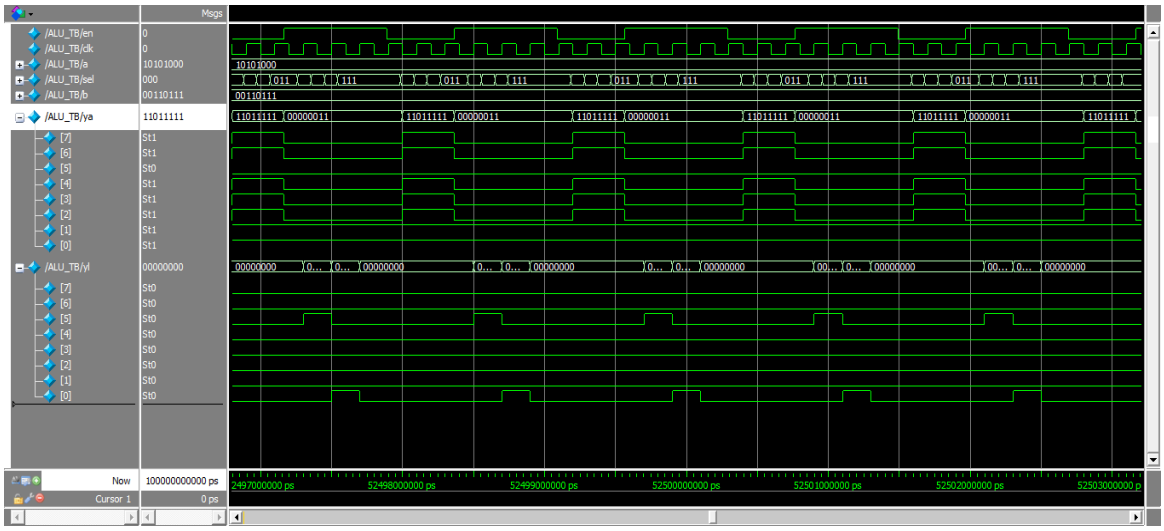


Figure .10: Waveform simulation of ALU with tri logic

B- **Power Consumption Results**

The 130 nm technology library is used to calculate power consumption of design. The circuit is operated at different frequencies and power consumption is noted accordingly as shown in the table 2 and 3. It's clear from table 3 and figure 11 that, the main part affecting to the power consumption is the dynamic power. There are a little bit differences between dynamic power and total power consumption. Where, in traditional state the two modules of ALU switch ON but one module only gives the target output. While the using of a new suggestion technique made one module switch OFF. Then only target part switched ON to give the output. The advantage for this technique observed from the compression between table 2 and table 3 the reason for that of reducing in switching activities inside ALU. Figure 11 shows the effecting of three types of power consumption to see which one is the most effecting power.

Table .2: Type of power consumption in ALU without using tri-state logic

Frequency MHz	Time ns	Dynamic Mw	Leakage Mw	Total Mw
100	10	0.2036	0.0007	0.2044
200	5	0.5246	0.0012	0.5259
300	3.3333	0.8975	0.0014	0.8990
500	2	1.5766	0.0014	1.5781
800	1.25	2.5003	0.0013	2.5017
1000	1	3.1115	0.0013	3.1128

Table .3: Type of power consumption in ALU using tri-state logic

Frequency MHz	Time ns	Dynamic Mw	Leakage Mw	Total Mw
100	10	0.1658	0.0014	0.1670
200	5	0.4330	0.0014	0.4345
300	3.3333	0.6420	0.0013	0.6435
500	2	1.0992	0.0013	1.1006
800	1.25	1.7264	0.0013	1.7278
1000	1	2.0894	0.0013	2.0908

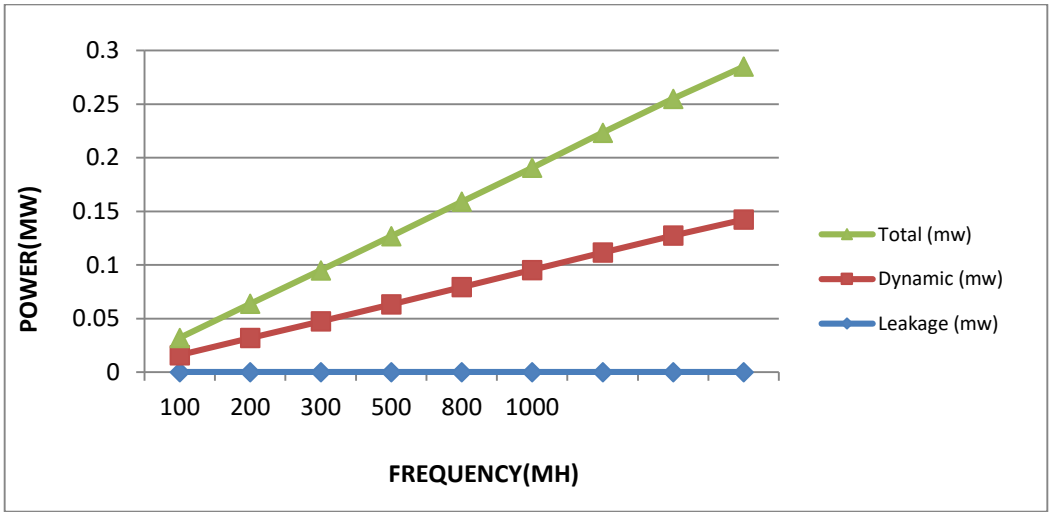


Figure .11: The difference between various types of power consumption

C- **Resource Utilization**

In table 3, resource utilization summary is shown. In this research paper, tri-state logic is used for control 8-bit of ALU design. In this technique, arithmetic operations are implemented. Moreover, logic operations are achieved too. This will lead to less resource usage. After the compilation, synthesis is performed. Quartus II 14.1 (64-bit) Web Edition illustrated RTL schematic of ALU. The RTL schematic is obtained, the device utilization of the design of ALU with tri-state logic is tabulated in table 4.

Table .4: Device Utilization with tri state logic

Recourses	Used	Available	Utilized%
Total logic elements	174	14,400	1%
Total combinational functions	174	14,400	1%
Dedicated logic registers	16	14,400	<1%
Total registers	16		
Total pins	37	81	46%

4. CONCLUSION

Last of all in this research we have a new design that will save more power. The key contribution of this paper is to develop a new clock signal technique and improve the performance of the digital circuit. The increase in dynamic power consumption makes the system unreliable, so to control the dynamic switching power various techniques are studied and analyzed to reduce it. A new tri-state based clock technique is proposed with low power dissipation. Comparative analysis shows that the proposed technique impacts on the dynamic power. All the analyses are done on an 8 bit ALU with process variation parameters. Improving ALU can significantly optimize the performance of processor. As concluded from power report summarized in table 3, by disabling the inactive blocks, dynamic power dissipation can be significantly decreased. This fulfilled the purpose of this wok, reduction in power consumption. Finally, the performance evaluation of the various modules is carried out using Synopsys tools and it is found that, the circuits designed using tir-state logic showed a reduced power. As a future work a reversible divider can also be designed and included into this ALU.

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